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| EXAMINER | |
|---|---|
| GETACHEW, ABIY | |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/840,051 | BOTHE ET AL. | |
| | Examiner | Art Unit | |
| | ABIY GETACHEW | 2841 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *10 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-15 and 17-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 17-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1,2,3,4,15,18,21,22,23,24 and 25 are rejected under 35 U.S.C. 102(b) as being by Sato et al. (4,712,160)

Regarding claim 1 Sato et al discloses a power supply circuit (Figure 1B) comprising at least one transformer (3) which is connected to a primary side circuit (1) and to a secondary side circuit (2), wherein the primary side circuit (1) and the secondary side circuit (2) are each mounted on at least one separate circuit carrier (4), said circuit carriers (4) being mechanically and electrically coupled with one another and arranged in at least two different planes.[Column 3 paragraph 3 lines 37-45] wherein the plane defined by the at least one secondary side (2) circuit carrier extends in a direction substantially transverse to the plane defined by the at least one primary side circuit carrier (4), and wherein the at least one primary side circuit carrier (4) is separated by an electrically insulating layer from the at least one secondary side circuit carrier (4).

Regarding claim 2 as applied claim 1 above Sato et al. discloses A power supply circuit (Figure 1B) comprising at least one transformer (3) which is connected to a primary side circuit and to a secondary side circuit (2), wherein the primary side circuit

and the secondary side circuit are each mounted on at least one separate circuit carrier (4), said circuit carriers (4) being mechanically and electrically coupled with one another and arranged in at least two different planes. Wherein the plane defined by the at least one secondary side (2) circuit carrier (4) extends in a direction substantially transverse to the plane defined by the at least one primary side (1) circuit carrier (4). (See figure 1B)

Regarding claim 3 as applied claim 1 above Sato et al. discloses, wherein the primary side circuit (1) is mounted on a plurality of primary side circuit carriers (See figure 1B) the planes of which are substantially in parallel with one another (See figure 1B).

Regarding claim 4 as applied claim 1 above Sato et al. discloses, wherein the at least one primary side circuit carrier (4) is separated by an electrically insulating layer from the at least one secondary side circuit carrier (4). (See figure 1B element (9) i.e. the thermal conduction between the two circuit boards is also reduced by the clearances (9))

In regards to claim 15 as applied claim 1 above Sato et al. discloses, wherein the transformer (3) is an electromagnetic transformer (3) (See figure 1B) [Electromagnetism is the physics of the electromagnetic field: a field, encompassing all of space, composed of the electric field and the magnetic field. The electric field can be produced by stationary electric charges, and gives rise to the electric force, which causes static electricity and drives the flow of electric current in electrical conductors]

In regards to claim 18 as applied claim 1 above Sato et al. discloses, wherein at least one of the circuit carriers (4) is designed such that it discharges dissipated heat (See figure 2) produced during operation to the outside.

In regards to claim 21 as applied claim 1 above Sato et al. discloses wherein it is surrounded at least in part by an electrically insulating coating. [See the abstract, i.e. an integral module by a resin of high thermal conduction and electrical insulation properties, the device-mounted sides of the primary and secondary circuit boards facing each other]

In regards to claim 22, as applied claim 21 above Sato et al. discloses, wherein the electrically insulating coating is formed by a casting material. [Column 6 paragraph 7 lines 36-43]

In regards to claim 23 and 24, as applied claim 15 above Sato et al. discloses, wherein electrical components (5 and 6) are integrated into a coil body of the transformer. (Referring to FIGS. 1(A) and 1(B): (1) is a primary circuit board on which the components of group A of FIG. 2 are integrated on one side; (2) is a secondary circuit board on which the components of group B of FIG. 2 are integrated on one side; (3) is a converter transformer; (4) is an electrical insulation material for joining the entire module)

In regards to claim 25, Sato et al. discloses, A method for producing a power supply circuit (See figure 1B) comprising at least one transformer (3), a primary side circuit (1) and a secondary side circuit (2), said method comprising the following steps: mounting the primary side circuit (1) on at least one primary side circuit carrier mounting (4) the

secondary side circuit (2) on at least one separate secondary side circuit carrier (7) electrically and mechanically coupling the circuit carriers (7) with the transformer, the circuit carriers (7) being arranged in at least two different planes (See the Abstract) and wherein the plane defined by the at least one secondary side (2) circuit carrier extends in a direction substantially transverse to the plane defined by the at least one primary side circuit carrier (4), and wherein the at least one primary side circuit carrier (4) is separated by an electrically insulating layer from the at least one secondary side circuit carrier (4)

In regards to claim 26, Sato et al. discloses a method for producing a power supply circuit (See figure 1B) comprising at least one transformer (3), a primary side circuit and a secondary side circuit, said method comprising the following steps: mounting the primary side circuit (1) on at least one primary side circuit carrier (7); mounting the secondary side circuit (2) on at least one separate secondary side circuit carrier (7); and electrically and mechanically coupling the circuit carriers with the transformer (3), the circuit carriers (4) being arranged in at least two different planes, wherein the primary side circuit is mounted on a plurality of primary side circuit carriers (7) , the planes of which are substantially in parallel with one another.

Claim 5-14,17,19 and 20 are rejected under 103 (a) Sato et al. (4,712,160) in view of Bujatti et al. (4,925,723)

Regarding claim 5 as applied claim 1 above Sato et al. discloses, wherein at least one of the circuit carriers (4) circuit carriers comprises integrated resistors which can preferably be produced by thick film technology.

Bujatti et al. does not expressly disclose integrated resistors, which can preferably be produced by thick film technology.

Sato et al. discloses integrated resistors (14), which can preferably be produced by thick film technology [Column 1 paragraph 3 lines 42-48].

Sato et al. and Bujatti et al. are analogous art and both arts in the same area of invention, manufacturing of integrated circuits formed on a substrate or circuit carrier.

At the time of the invention it would have been obvious to combine Sato et al. and Bujatti et al. to obtain direct connections between specific points of the circuit on the upper surface and the metallization on the lower surface. So therefore, it would have been obvious to combine Sato et al. and Bujatti et al. in order to obtain integrated circuits formed on a substrate or circuit carrier.

In regards to claim 6, as applied claim 1 above Sato et al. discloses. Wherein at least one of the circuit carriers (4) circuit carriers comprises integrated capacitors of a medium dielectric strength.

Bujatti et al. discloses integrated capacitors (14) of a medium dielectric strength [Column 3 paragraph 3 lines 13-21] [Examiner's interpretation of medium dielectric strength is as the value of a material as an electrical insulator or the resistance to the flow of electric current.

Sato et al. and Bujatti et al. are analogous art and both arts in the same area of invention, manufacturing of integrated circuits formed on a substrate or circuit carrier.

At the time of the invention it would have been obvious to combine Sato et al. and Bujatti et al. in order to obtain direct connections between specific points of the

circuit on the upper surface and the metallization on the lower surface. So therefore, it would have been obvious to combine Sato et al. and Bujatti et al. in order to obtain integrated circuits formed on a substrate or circuit carrier.

In regards to claim 7, as applied claim 1 above Sato et al. discloses, wherein the integrated capacitors can be produced as a monolayer structure. (See figure 1B)

Sato et al. does not expressly disclose integrated capacitors.

Bujatti discloses wherein the integrated capacitors (14).

Sato et al. and Bujatti et al. are analogous art and both arts in the same area of invention, manufacturing of integrated circuits formed on a substrate or circuit carrier.

At the time of the invention it would have been obvious to combine Sato et al. and Bujatti et al. in order to obtain direct connections between specific points of the circuit on the upper surface and the metallization on the lower surface. So therefore, it would have been obvious to combine Sato et al. and Bujatti et al. in order to obtain integrated circuits formed on a substrate or circuit carrier.

In regards to claims 8 and 12 as applied claim 6 above Sato et al. discloses, wherein circuit carriers (4) circuit carriers comprises integrated capacitors of a medium dielectric strength.

Sato et al. does not disclose the integrated capacitors can be produced as a multilayer structure.

Bujatti et al. disclose the integrated capacitors can be produced as a multilayer structure. [Column 2 paragraph 4 lines 15-20]

Sato et al. and Bujatti et al. are analogous art and both arts in the same area of invention, manufacturing of integrated circuits formed on a substrate or circuit carrier.

At the time of the invention it would have been obvious to combine Sato et al. and Bujatti et al. to obtain direct connections between layers. So therefore, it would have been obvious to combine Sato et al. and Bujatti et al. to obtain integrated circuits formed on a substrate or circuit carrier.

In regards to claims 9 and 13 as applied claim 6 above Sato et al. discloses, wherein circuit carriers (4)

Sato et al. does not disclose wherein the integrated capacitors can be produced by introducing a dielectric precursor into recesses.

Bujatti et al. disclose wherein the integrated capacitors (14) can be produced by introducing a dielectric precursor (See figure 2C element 23) into recesses (16).

Sato et al. and Bujatti et al. are analogous art and both arts in the same area of invention, manufacturing of integrated circuits formed on a substrate or circuit carrier. So therefore, it would have been obvious to combine Sato et al. and Bujatti et al. in order to obtain integrated circuits formed on a substrate or circuit carrier.

In regards to claim 10 and 14 as applied claim 1 above Sato et al. discloses, wherein at least one of the circuit carriers (4)

Sato et al. does not expressly disclose integrated capacitors of a high dielectric strength.

Bujatti et al. discloses integrated capacitors (14) of a high dielectric strength [Column 3 paragraph 3 lines 13-21] [Examiner's interpretation of medium dielectric

strength is as the value of a material as an electrical insulator or the resistance to the flow of electric current.

Sato et al. and Bujatti et al. are analogous art and both arts in the same area of invention, manufacturing of integrated circuits formed on a substrate or circuit carrier.

At the time of the invention it would have been obvious to combine Sato et al. and Bujatti et al. in order to obtain direct connections between specific points of the circuit on the upper surface and the metallization on the lower surface. So therefore, it would have been obvious to combine Sato et al. and Bujatti et al. in order to obtain integrated circuits formed on a substrate or circuit carrier.

In regards to claim 11 as applied claim 10 above Sato et al. discloses, a monolayer structure (See figure 1B).

Sato et al. does not expressly disclose the integrated capacitors.

Bujatti et al. discloses integrated capacitors (14)

Sato et al. and Bujatti et al. are analogous art and both arts in the same area of invention, manufacturing of integrated circuits formed on a substrate or circuit carrier.

At the time of the invention it would have been obvious to combine Sato et al. and Bujatti et al. to obtain integrated capacitors can be produced as monolayer structure. So therefore, it would have been obvious to combine Sato et al. and Bujatti et al. to obtain integrated circuits formed on a substrate or circuit carrier as monolayer structure.

In regards to claim 17 as applied claim 1 above Sato et al. discloses, wherein at least one of the circuit carriers (4)

Sato et al. does not expressly disclose circuit carriers produced from a ceramic material.

Bujatti et al. discloses substrate produced from a ceramic material. [Column 1 paragraph 2 lines 15-25]

Sato et al. and Bujatti et al. are analogous art and both arts in the same area of invention, manufacturing of integrated circuits formed on a substrate or circuit carrier.

At the time of the invention it would have been obvious to combine Sato et al. and Bujatti et al. to manufacturing of integrated circuits formed on a substrate or circuit carrier. So therefore, it would have been obvious to combine Sato et al. and Bujatti et al. to obtain circuit carriers produced from a ceramic material.

In regards to claim 19, as applied claim 1 above Sato et al. discloses, wherein the individual circuit carriers (4)

Sato et al. does not expressly disclose mechanically connectable to one another by means of joint sintering, adhesive bonding or soldering.

Bujatti et al. discloses mechanically connectable to one another by means of joint sintering, adhesive bonding or soldering. [Column 3 paragraph 2 lines 5-12]

Sato et al. and Bujatti et al. are analogous art and both arts in the same area of invention, manufacturing of integrated circuits formed on a substrate or circuit carrier.

At the time of the invention it would have been obvious to combine Sato et al. and Bujatti et al. in order to obtain connections between specific points of the circuit on the upper surface and the metallization on the lower surface by means of joint adhesive. So therefore, it would have been obvious to combine Sato et al. and Bujatti et al. in order to

mechanically connectable to one another by means of joint sintering, adhesive bonding or soldering.

In regards to claim 20, as applied claim 1 above Sato et al. discloses, wherein the individual circuit carriers are electrically connectable to one another through vias in at least one insulation layer.

Sato et al. does not expressly discloses mechanically connectable to one another by means of joint sintering, adhesive bonding or soldering.

Bujatti et al. discloses mechanically connectable to one another by means of joint sintering, adhesive bonding or soldering. [Column 1 paragraph 2 lines 15-35]

Sato et al. and Bujatti et al. are analogous art and both arts in the same area of invention, manufacturing of integrated circuits formed on a substrate or circuit carrier.

At the time of the invention it would have been obvious to combine Sato et al. and Bujatti et al. in order to obtain connections between specific points of the circuit on the upper surface and the metallization on the lower surface by means of cutting holes, referred in the teaching as “Via holes” So therefore, it would have been obvious to combine Sato et al. and Bujatti et al. in order to obtain mechanically connectable to one another by means of joint sintering, adhesive bonding or soldering.

***Response to Arguments***

1. Applicant's arguments filed on 10/12/2007 have been fully considered but they are not persuasive.

First, Applicant argue "Sato does not disclose a power supply circuit comprising at least one transformer which is connected to a primary side circuit and to a secondary side circuit"

**Examiner Disagree:** Because Sato et al. disclose a primary circuit board on one side of which a part of the primary circuit of a switching power supply unit is integrated, and a secondary circuit board on one side of which a part of the secondary circuit of the switching power supply unit is integrated are three-dimensionally joined into an integral module by a resin of high thermal conduction and electrical insulation Properties. Sato does disclose a power supply circuit comprising at least one transformer which is connected to a primary side circuit and to a secondary side circuit, Applicant's attention respectfully directed to figure 1B, i.e. circuit boards (1) are arranged so that the sides on which devices (5) and (6) are mounted, respectively, face each other, and transformer (3) is placed between circuit boards (1) and (2). Circuit boards (1) and (2) and the transformer (3), thus arranged, are entirely and three-dimensionally joined by the resin (4) into an integral module. The primary side circuit (1) and the secondary side circuit (2) are each mounted on at least one .separate circuit carrier (4), said circuit carriers (4) being mechanically and electrically coupled with one another and arranged in at least two different planes.[Column 3 paragraph 3 lines 37-45]

Second, "Bujatti does not disclose a power supply circuit comprising at least one transformer which is connected to a primary side circuit and to a secondary side circuit"

**Examiner Disagree:** because Bujatti teaches that in the manufacturing of a power supply circuit formed on a substrate, there is a direct connection between the circuit on the primary side circuit and the secondary side circuit. Bujatti also teaches that such connections may be required for two different reasons:

(1) To create a low inductance/low resistance path to ground; and

(2) To provide an effective heat sinking, specifically for active devices. In the present state of the art when the substrate used is a ceramic substrate, such connections are typically obtained by cutting holes, referred to as "via holes" or "vias", through the substrate and by metallizing the wall of the holes. Applicant attention respectfully directed to the Abstract.

***Conclusion***

2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ABIY GETACHEW whose telephone number is (571)272-6932. The examiner can normally be reached on Monday to Friday 8Am to 4:30Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DEAN REICHARD can be reached on (571)272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dean A. Reichard/
Supervisory Patent Examiner, Art Unit 2841

Abiy Getachew
Examiner
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A.G.
March 14, 2008